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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/502,994	02/11/2000	Michael Mantor	11142	5992

7590 09/20/2002

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EXAMINER
WALLACE, SCOTT A

ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 09/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/502,994	MANTOR ET AL.	
	Examiner	Art Unit	
	Scott Wallace	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18* is/are allowed.

6)☒ Claim(s) *2-10,13,14 and 19* is/are rejected.

7)☒ Claim(s) *12 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The indicated allowability of claim 14 is withdrawn in view of the newly discovered reference(s) to Wang et al. U.S. Patent No. 5,831,640. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al., U.S. Patent No. 5,831,640 in view of Schilling et al., U.S. Patent No. 6,236,405.

4. As per claim 14, Wang et al. discloses a computer graphics processor system (col. 5 lines 15-16, 40-45, 33-37) having the capability of mapping texture (col. 6 lines 14-17) onto a three dimensional object in a scene being displayed (col. 5 lines 33-37), the system comprising:

a texture address calculator (fig. 3 element 220) for generating texel addresses for a list of primitives being processed (col. 7 lines 1-5, 12-15, 20-23).

a texture cache controller (fig. 3, element 250) for determining and requesting the necessary transfer of texels from said texture main memory (fig. 3 element 102) addresses to said texture cache memory (fig 3 element 251) addresses ((col. 7 lines 55-58 and col. 8 lines 2-5)(cache controller circuits and techniques are well known in the art)).

a texture cache arbiter (fig 3 controller circuit 250) for scheduling controlling the actual transfer of texels from said texture main memory into the texture cache memory ((col. 8 lines 2-5)(memory arbiters used to control fetching and transfer of data between memories are well known in the art and can be considered a part of a cache controller)).

a texture cache arbiter (250) for controlling the outputting of texels for each pixel to an interpolating filter (260) from the cache memory ((col. 8 lines 30-3 (cache controller circuit

includes cache memory (fig 3)), col. 9 lines 60-63)(linear, bilinear, and trilinear filtering are well known in the art as interpolation filtering techniques)).

a cache arbiter coupled between said controller and said texture cache memory (fig 3) for determining which texels in the cache memory can be overwritten when new texels are determined to be transferred to said cache memory by said cache controller (col. 8 lines 12-28 and 47-63).

Wang et al. Fails to dislcose :

A texture main memory containing an array of texels, each texel having an address and one of N identifiers.

A texture cache memory having addresses partitioned into N banks, each bank containing texels transferred from said main memory that have the corresponding identifier.

However, Schilling et al. from a similar field of endeavor discloses these limitations as described above. Refer to fig 2 and col. 4 lines 15-19 for the first limitation and col. 4 lines 15-19 for the second limitation. Fig. 2 shows an array of texels with each texel having one of four identifiers. Each 2x2 group of texels with identifiers 1,2,3,4 are assigned to memory banks 1,2,3 and 4 respectively.

It would have been obvious to a person of ordinary skill in the art to incorporate the texture mapping system of Schilling et al. into the Wang et al. texture mapping system to provide a texture mapping system with high rendering speeds. Furthermore, such a texture mapping system would reduce the amount of data to be stored and accessed by a texture mapping system as suggested by Schilling et al. (col. 2 lines 1-4, 28-29).

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. in view of Schilling et al. in further in view of Chard et al., U.S. Patent No. 5,809,280.

6. As per claim 19, Wang et al. discloses a computer graphics processor system (col. 5 lines 15-16, 40-45, 33-37) having the capability of mapping texture (col. 6 lines 14-17) onto a three dimensional object in a scene being displayed (col. 5 lines 33-37), the system comprising:

a texture address calculator (fig. 3 element 220) for generating texel addresses for a list of primitives being processed (col. 7 lines 1-5, 12-15, 20-23).

a texture cache controller (fig. 3, element 250) for determining and requesting the necessary transfer of texels from said texture main memory (fig. 3 element 102) addresses to said texture cache memory (fig 3 element 251) addresses ((col. 7 lines 55-58 and col. 8 lines 2-5)(cache controller circuits and techniques are well known in the art)).

a texture cache arbiter (fig 3 controller circuit 250) for scheduling controlling the actual transfer of texels from said texture main memory into the texture cache memory ((col. 8 lines 2-5)(memory arbiters used to control fetching and transfer of data between memories are well known in the art and can be considered a part of a cache controller)).

a texture cache arbiter (250) for controlling the outputting of texels for each pixel to an interpolating filter (260) from the cache memory ((col. 8 lines 30-3 (cache controller circuit includes cache memory (fig 3)), col. 9 lines 60-63)(linear, bilinear, filtering techniques)).

a cache arbiter coupled between said controller and said texture cache memory (fig 3) for determining which texels in the cache memory can be overwritten when new texels are determined to be transferred to said cache memory by said cache controller (col. 8 lines 12-28 and 47-63).

Wang et al. Fails to dislcose :

A texture main memory containing an array of texels, each texel having an address and one of N identifiers.

A texture cache memory having addresses partitioned into N banks, each bank containing texels transferred from said main memory that have the corresponding identifier.

However, Schilling et al. from a similar field of endeavor discloses these limitations as described above. Refer to fig 2 and col. 4 lines 15-19 for the first limitation and col. 4 lines 15-19 for the second limitation. Fig. 2 shows an array of texels with each texel having one of four identifiers. Each 2x2 group of texels with identifiers 1,2,3,4 are assigned to memory banks 1,2,3 and 4 respectively.

It would have been obvious to a person of ordinary skill in the art to incorporate the texture mapping system of Schilling et al. into the Wang et al. texture mapping system to provide a texture mapping system with high rendering speeds. Furthermore, such a texture mapping system would reduce the amount of data to be stored and accessed by a texture mapping system as suggested by Schilling et al. (col. 2 lines 1-4, 28-29).

Wang et al and Schilling et al together fail to disclose said cache controller including a plurality of least recently used controllers coupled in succession to thereby transfer texels according to a least recently used replacement algorithm. Chard et al. Discloses this in the abstract and col. 1 lines 63-67 and col. 2 lines 1-10. Chard et al. Does not specifically use texels, but uses any type of data which could be texels to show using a plurality of LRUs is used to improve the overall performance of this type of enviroment. It would have been obvious to one of ordinary skill in the art to use the plurality of LRUs of Chard et al with the combined system of Wang and Schilling because this would have improved the read-ahead performance of the combined system (col. 20 lines 19-35).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Scott Wallace** whose telephone number is **703-605-5163**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Michael Razavi**, can be reached at 703-305-4713.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600